

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A processing device comprising:
2 a processing module capable of multitasking multiple tasks;
3 one or more associated circuits, which may be selectively
4 configured responsive to control signal, coupled to said processing
5 module for supporting the processing module, said one or more
6 associated circuits includes a cache configuration circuitry for
7 configuration of a cache; and
8 a memory storing a ~~control word~~ task attribute bits for
9 configuring the ~~associated circuits~~ cache via the cache
10 configuration circuitry, wherein each task has an associated
11 ~~control word~~ task attribute bit which is stored in the memory while
12 the task is being executed by the processing module.

1 2. (Currently Amended) The processing device of claim 1
2 wherein said ~~control word~~ task attribute bits comprises a plurality
3 of fields.

1 3. (Original) The processing device of claim 2 wherein each
2 of said associated circuits has an associated field.

1 4. (Original) The processing device of claim 3 wherein each
2 of said associated circuits has configuration circuitry for
3 configuring the associated circuit responsive to a value stored in
4 said associated field.

Claims 5 to 13. (Canceled)

1 14. (Original) The processing device of claim 1 wherein said
2 processing module comprises a first processing module, and further
3 comprising one or more additional processing modules.

1 15. (Currently Amended) A method of operating a processing
2 device including a processing module capable of multitasking
3 multiple tasks coupled to one or more associated circuits, said one
4 or more associated circuits includes a cache configuration
5 circuitry for configuration of a cache, comprising the steps of:
6 identifying a current task; and
7 storing ~~a control word~~ task attribute bits associated with
8 said current task in a memory; and
9 configuring the ~~associated circuits~~ cache circuitry via the
10 cache configuration circuitry to a state responsive to the ~~control~~
11 ~~word~~ task attribute bits during execution of said current task.

1 16. (Currently Amended) The method of claim 15 wherein said
2 storing step comprises the step of storing ~~a control word~~ task
3 attribute bits having a plurality of predefined fields.

1 17. (Currently Amended) The method of claim 16 wherein each
2 of said associated circuits has an associated field in said ~~control~~
3 ~~word~~ task attribute bits.

1 18. (Original) The method of claim 17 wherein said enabling
2 or disabling step comprises the step of configuring each of the
3 associated circuits responsive to a value stored in said associated
4 field.

Claims 20 to 23. (Canceled)

1 24. (Currently Amended) The method of claim 15 wherein said
2 processing module includes a plurality of processing subsystems and
3 further comprising the step of configuring said processing
4 subsystems responsive to said ~~control word~~ task attribute bits.

Claims 25 and 26. (Canceled)

1 27. (New) The processing device of claim 1, wherein:
2 said cache includes a plurality of selectively configurable
3 cache ways; and
4 said cache configuration circuitry configures said cache ways
5 according to said task attribute bits.

1 28. (New) The processing device of claim 1, wherein:
2 said cache includes a plurality of selectively configurable
3 data paths; and
4 said configuration circuitry configures said cache data paths
5 according to said task attribute bits.

1 29. (New) The method of claim 15, wherein:
2 said step of configuring the cache circuitry via the cache
3 configuration circuitry configures cache ways according to the task
4 attribute bits.

1 30. (New) The method of claim 15, wherein:
2 said step of configuring the cache circuitry via the cache
3 configuration circuitry configures cache data paths according to
4 said task attribute bits.